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# PRE-APPEAL BRIEF REQUEST FOR REVIEW

| Docket Number (Optional) |
|---|
| iSPHERES 7 |

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

on March 05, 2008

Signature Theresa Belich

Typed or printed name Theresa L. Belich

| Application Number | Filed |
|---|---|
| 10/775,745 | Feb. 9, 2004 |

| First Named Inventor |
|---|
| Eric T. Bax |

| Art Unit | Examiner |
|---|---|
| 2164 | S. Pannala |

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant/inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [XX] attorney or agent of record. Registration number 29,355
- [ ] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

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05 March 2008
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

[XX] *Total of 03 forms are submitted. (Notice, Request, Pre-Appeal Brief Req.)

IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

**Patent Application**

Inventors: **Eric T. Bax**

Case No.: **iSpheres 7**

Serial No.: **10/775,745** Group Art Unit: **2164**

Filing Date: **February 9, 2004**

Examiner: **Sathyanaraya R. Pannala**

Title: **Finite-State Machine Augmented For Multiple Evaluations of Text**

Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

## PRE-APPEAL BRIEF REQUEST FOR REVIEW

SIR:

The Examiner rejected claims 1-3 and 5 under 35 U.S.C. §103 over U.S. patent no. 7,072,880 (Beesley) in view of U.S. patent no. 5,630,130 (Perotto et al.). This rejection is traversed.

By way of brief background, a counter is employed to determine relevance (correspondence) of a character sequence that is associated with the counter (a "pattern") to some other character sequence (a "text"). Counter evaluation – computing the counter score for a text – is performed using a finite-state machine that transitions from state to state based on the sequence of characters in the text. Each state has a value. A multi-counter contains a set of counters. Computing the multi-counter score for a text is called multi-counter evaluation. Multi-counter evaluation evaluates the relevance of a text to multiple patterns. The score of a multi-counter for a text comprises the scores for the individual counters of the multi-counter.

The claimed invention is directed to multi-counter evaluation. According to the claims, multi-counter evaluation is performed using a

merged finite-state machine that represents the finite-state machines of the individual counters of the multi-counter. The merged finite-state machine is augmented with state value lists instead of state values. Each state value list indicates which counter scores receive which values for the corresponding state.

Applicant's claims recite that a merged machine represents a plurality of single-counter finite-state machines each representing a different one of a plurality of counters and wherein at least one state of the merged finite-state machine each corresponds to a multiplicity of states each of a different one of said single-counter finite-state machines. Claim 1 recites a "merged finite-state machine... wherein at least one state of the merged finite-state machine each corresponds to a multiplicity of states each of a different one of said single-counter finite-state machines, augmented with state value lists where each state value list indicates which counter... receives which value for the state of the merged finite-state machine". Claim 2 recites "a merged finite-state machine... wherein at least one state of the merged finite-state machine each corresponds to a multiplicity of states each of a different one of said single-counter finite-state machines, augmented with state value lists where each state value list indicates which patterns in which counters... are found when the state of the merged finite-state machine is entered". Claim 3 recites "accumulating... to form a merged machine... wherein at least one state of the merged finite-state machine each corresponds to a multiplicity of states each of a different one of a said single-counter finite-state machines, including converting state values of states of the finite-state machines... into state value lists of states of the merged machine." Claim 5 recites "providing the augmented finite-state machine... wherein at least one state of the augmented finite-state machine each corresponds to a multiplicity of states each of a different one of said single-counter finite-state machines," and "forming a state value list if the final state lacks a

state value list, forbearing from forming a state value list if the final state has a state value list, and adding to the state value list a reference to the counter and the pattern value."

In contrast, Beesley discloses a transducer/acceptor/network that comprises a plurality of state machines that are strung together serially (see, e.g., Fig. 11). The transducer/acceptor/network corresponds to strings/words, while each state machine corresponds to a domain of sub-strings/formants. Since the transducer/acceptor/network is a concatenation of finite-state machines, the transducer/acceptor/network does not have at least one state each corresponding to a multiplicity of states each of a different one of the finite-state machines. Consequently, the transducer/acceptor/network is also not augmented with state value lists – the concept of a state value list is not applicable to the structure of a transducer/acceptor/network of Beesley.

The Examiner pointed to Figs. 13 and 14, col. 13, lines 56-67, and col. 14, lines 16-24 and 30-33 of Beesley as teaching a merged or augmented finite-state machine having at least one state each corresponding to a multiplicity of states each of a different one of the single-counter finite state machines and augmented with state value lists. The Examiner is mistaken. These figures and passages set forth steps for the preparation and use of a network for substring-to-number mapping and for retrieving related information, and not what the Examiner purports.

The Examiner did concede that "Beesley does not explicitly teach using multi-counters," and cited Perotto et al. for this teaching. But the combination of Beesley and Perotto et al. likewise fails to teach applicant's claimed invention.

Perotto et al. disclose a multitasking controller that has a separate program counter, a separate accumulator, and a separate index register, for each one of a plurality of tasks. Thus, there is a bank of a plurality of individual program counters, another bank of a plurality of individual

accumulators, and another bank of a plurality of individual index registers. A program counter points to a memory location containing the next instruction that is to be executed of its corresponding task (column 4, lines 4-6). An accumulator holds data associated with its corresponding task for use by the arithmetic and logic unit (column 5, lines 31-34). An index register stores an address employed by its corresponding task as an offset value for indexed addressing (column 5, lines 1-2 and 38-40).

Perotto et al. bear no relation either to Beesley or to applicant's claimed invention. Perotto et al. are concerned with efficient operation of a multitasking controller, and not with the substring-number mapping of Beesley or with multi-counter evaluation like applicant. Nor do Perotto et al. disclose a multi-counter, as is made evident by the above discussion of the disclosure of Perotto et al.

Nevertheless, even if one assumes for purposes of argument that Perotto et al. do disclose a multi-counter, Perotto et al. still fail to cure the fundamental failure of Beesley to disclose, teach, or suggest the claimed invention. Specifically, the combined teachings of Beesley and Perotto et al. fail to disclose, teach, or suggest a merged or augmented finite-state machine as defined in the claims, or at least a state-value list and augmentation therewith of the merged or augmented finite-state machine, as is required by the recitations of all of applicant's claims.

Examiner summarily dismissed applicant's explanation by saying that "Applicant's arguments fail to comply with 37 CFR 1.11(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references."

This cursory dismissal is, at best, disingenuous. Applicant has explained at length why the combined teachings of the applied references "fail to disclose, teach, or suggest a merged or augmented finite-state machine as defined in the claims, or at least a state-value list and

augmentation therewith of the merged or augmented finite-state machine, as is required by the recitations of all of applicant's claims," and has pointed out and quoted the specific recitations of the claims that distinguish his invention from the applied references. How much more specific could applicant be?

Other than nakedly asserting that certain passages of Beesley and Perotto et al. teach the claimed matter, the Examiner has provided no explanation for his assertion of obviousness. Nor has the Examiner rebutted applicant's contrary position. This is insufficient to establish obviousness. "[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." KSR Int'l. v. Teleflex Inc., 550 U.S. ____ (2007), citing In re Kahn, 441 F. 3d 977, 988 (Fed. Cir. 2006). Hence, the Examiner has failed to establish obviousness of applicant's claimed subject matter.

For the reasons given above, applicant asserts that the combined teachings of Beesley and Perotto et al. do not render applicant's claims unpatentable. Applicant therefore requests that the Section 103(a) rejection of his claims 1-3 and 5 be withdrawn.

Respectfully submitted,
**Eric T. Bax**

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Date: 05 March 2008

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